CBCS SCHEME

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15EC663

Sixth Semester B.E. Degree Examination, Feb./Mar.2022
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Assuming 2 vats in a factory, write the verilog code for a vat buzzer to maintain the temperature between 25˚C and 30˚C. The buzzer should be activated if the temperature is too high or too low or the vat level is too low. A switch provided helps in selecting any one vat at any time. Draw the buzzer circuit. **(08 Marks)**

b. Develop a verilog code for a 7-segment decoder. Include an additional input "Blank" thtat overrides the BCD input and causes all segments not to be lit. Explain the code. **(08 Marks)**

OR

2 a. What is meant by design methodology? Explain the basic steps of design methodology, in brief. **(08 Marks)**

b. Design a control sequence for the control signals of the sequential complex multiplier. **(08 Marks)**

Module-2

3 a. Design 512 $K \times 32$ bit memory using 512 $K \times 8$ bit memory components. **(08 Marks)**

b. Design a circuit that computes the function $y = ci \times x^2$, where x is a binary coded input value and Ci is a coefficient stored in a flow-through SSRAM. x, Ci and y are all signed fixed-point valves with 8 pre-binary point and 12 post binary point bits. The index i is also an input to the circuit, encoded as a 12-bit unsigned integer, values for x and i arrive at the input during the cycle when a control input, start, is 1. The circuit minimize area by using a single multiplier to multiply Ci by x and then by x again. **(08 Marks)**

OR

4 a. Develop a verilog model for a dual-port, $4K \times 16$ bit flow-through SSRAM. One port allows data to be written and read, while the other port only allows data to be read. **(08 Marks)**

b. Explain soft errors and hard errors. Determine whether there is an error in the ECC word 000111000100 and if so correct if. **(08 Marks)**

Module-3

5 a. Explain the complex programmable logic devices (CPLDs). **(08 Marks)**

b. Explain types of PCB design. **(08 Marks)**

OR

6 a. Explain field-programmable gate arrays, in brief. **(08 Marks)**

b. Explain signal integrity interconnection issue in PCB design. **(08 Marks)**

Module-4

7 a. Briefly explain the serial interface standards for I/O devices. **(08 Marks)**

b. Explain Digital to Analog converter using R-string and explain its limitations. **(08 Marks)**

OR

8 a. Design an input controller that has 8-bit binary coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the Gummnut core when the input value changes. The controller is the only interrupt source in the system. Also develop verilog model for it. **(10 Marks)**

b. Explain the concept of tristate bus. **(06 Marks)**

Module-5

9 a. Explain the design flow of hardware/software codesign. **(08 Marks)**

b. Explain the term "Design optimization" highlighting on the area, timing and power optimization in brief. **(08 Marks)**

OR

10 a. With neat circuit diagram, explain 4 bit LFSR and 4 bit CFSR and their purpose. **(08 Marks)**

b. Write short note on scan design and boundry scan. **(08 Marks)**

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